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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,847	05/25/2001	Stefanos Kaxiras	Diodato 9-7-17-2	5066
7590 01/21/2005				
Ryan, Mason & Lewis, LLP 1300 Post Road, Suite 205 Fairfield, CT 06430		EXAMINER CAO, CHUN		
		ART UNIT PAPER NUMBER 2115		
DATE MAILED: 01/21/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/865,847	Applicant(s) KAXIRAS ET AL.	
	Examiner Chun Cao	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,9-17,20,21,23-29 and 31-35 is/are rejected.
- 7) ☒ Claim(s) 6-8,18,19,22 and 30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-35 are remained and presented for examination in this application.
2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.
3. Claims 1-5, 9, 10, 12-14, 17, 20, 21, 24, 27-28, 31, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wickeraad et al. (Wickeraad), US patent no. 6,490,654 in view of Bogin et al. (Bogin), U.S. Patent No. 5,835,435.

As per claim 1, Wickeraad discloses a cache memory [fig. 2], comprising:

a plurality of cache lines for storing a value from main memory [col. 1, lines 25-30; col. 4, lines 56-58]; and

a timer [counter] associated with each of said plurality of cache lines [col. 3, lines 30-33; col. 4, lines 58-61].

Wickeraad does not explicitly teach of using the timer configured to control signal that removes power to said associated cache line after a decay interval. In other words, Wickeraad fails to teach of powering down cache lines if the cache lines had not been accessed in a predetermine time period.

Bogin teaches of powering down cache lines if the cache lines had not been accessed in a predetermine time period [fig. 7; col. 2, lines 44-47col. 5, lines 21-49; col. 9, lines 19-44].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Wickeraad and Bogin because they both teach a cache memory system, the specific teachings of Bogin stated above would improve the

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efficiency of power consumption Wickeraad system by determining the activities of the cache lines.

As per claim 2, Wickeraad discloses a timer associated with a given cache line is reset each time said associated cache line is accessed [col. 3, lines 36-44].

As per claim 3, Wickeraad discloses that decay interval is variable [col. 3, lines 36-44].

As to claims 4 and 5, inherently, Bogin teaches that variable decay interval can be increased to increase performance and lowered to save power [col. 2, lines 50-61].

As per claim 9, Wickeraad discloses that a timer is a k bit timer and said timer receives a tick from any source [col. 3, lines 31-33].

As per claim 10, Wickeraad discloses that timer is any k-state finite state machine (FSM) that can function logically as a counter [fig. 2, col. 3, lines 31-33].

As per claim 13, Wickeraad discloses reset a valid field associated with cache line [col. 3, lines 36-44]. Bogin teaches of removing power from cache lines [col. 2, lines 44-47col. 5, lines 21-49; col. 9, lines 19-44].

As per claim 14, Bogin inherently teaches that a signal is configured to remove a potential from said cache line [col. 2, lines 44-47col. 5, lines 21-49; col. 9, lines 19-44].

As per claim 17, Wickeraad discloses a timer is an analog device [fig. 2, col. 3, lines 31-33].

As to claims 20, 21 and 24, Wickeraad and Bogin together teach the claimed system. Therefore Wickeraad and Bogin together teach the claimed method of steps to carry out the system.

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4. As to claims 27 and 28, Wickeraad discloses a plurality of cache lines for storing a value from main memory; and each of said cache lines comprised of one or more random access memory (RAM) cells and each of said RAM cells being refreshed each time said cache line is accessed, and a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period a timer [col. 1, lines 25-30; col. 3, lines 30-33; col. 4, lines 56-61].

Wickeraad does not explicitly teach of comprising of one or more dynamic random access memory (DRAM) cells.

Bogin discloses one or more dynamic random access memory (DRAM) cells [col. 4, lines 2-3].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Wickeraad and Bogin because the specific teachings of Stein stated above would improve the functionality Wickeraad system by using a DRAM cells to utilize the system.

As per claim 31, Wickeraad discloses that a timer is a k bit timer and said timer receives a tick from any source [col. 3, lines 31-33].

As per claim 32, Wickeraad discloses that timer is any k-state finite state machine (FSM) that can function logically as a counter [fig. 2, col. 3, lines 31-33].

As to claims 34 and 35, Wickeraad and Bogin together teach the claimed system. Therefore Wickeraad and Bogin together teach the claimed method of steps to carry out the system.

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5. Claims 11, 12, 16, 23, 26 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wickeraad et al. (Wickeraad), US patent no. 6,490,654 in view of Bogin et al. (Bogin), U.S. Patent No. 5,835,435 and Fuller (Fuller), U.S. Patent No. 5,632,038.

Fuller is a prior reference cited in prior office action.

As to claims 11, 23 and 33, Wickeraad and Bogin do not disclose a dirty bit associated with each of cache lines.

Fuller discloses a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval [col. 7, lines 28-38].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Wickeraad and Bogin and Fuller because the specific teachings of Fuller stated above would improve the reliability of Wickeraad system by backing up data prior to power is removed.

As per claim 12, Wickeraad discloses that one or more of said timer associated with plurality of cache lines are cascaded [fig. 2; col. 3, lines 31-33; col. 6, lines 7-22]. Fuller teaches of writing back to main memory [col.7, lines 28-38].

As to claims 16 and 26, Fuller inherently teaches of a first access to a cache line that has been powered down is delayed by a period of time that permits said cache line to stabilize after power is restored [col. 5, lines 36-48].

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6. Claims 15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wickeraad et al. (Wickeraad), US patent no. 6,490,654 in view of Bogin et al. (Bogin), U.S. Patent No. 5,835,435 and Takahashi (Takahashi), US patent no. 6,345,336.

As to claims 15 and 25, Wickeraad and Bogin both do not teach a first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line.

Takahashi teaches a first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line [col. 5, lines 36-48].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Wickeraad and Bogin and Takahashi because the specific teachings of Takahashi stated above would further improve the reliability Sherlock's system by restoring power to the cache lines.

7. Claims 27-29 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wickeraad et al. (Wickeraad), US patent no. 6,490,654 in view of Stein et al. (Stein), Session V: "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells" 1972, pages 56-57 and Fuller (Fuller), U.S. Patent No. 5,632,038.

As to claims 27 and 28, Wickeraad discloses a plurality of cache lines for storing a value from main memory; and each of said cache lines comprised of one or more random access memory (RAM) cells and each of said RAM cells being refreshed each

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time said cache line is accessed, and a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period a timer [col. 1, lines 25-30; col. 3, lines 30-33; col. 4, lines 56-61].

Wickeraad does not explicitly teach of comprising of one or more dynamic random access memory (DRAM) cells.

Stein discloses one or more dynamic random access memory (DRAM) cells [page 56, left column, paragraphs 1-2].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Wickeraad and Stein because the specific teachings of Stein stated above would improve the functionality Wickeraad's system by using a DRAM cells to utility the system.

As per claim 29, Stein discloses that DRAM cells are embodied as 4-T DRAM cells [page 56, left column, paragraph 1].

As per claim 31, Wickeraad discloses that a timer is a k bit timer and said timer receives a tick from any source [col. 3, lines 31-33].

As per claim 32, Wickeraad discloses that timer is any k-state finite state machine (FSM) that can function logically as a counter [fig. 2, col. 3, lines 31-33].

Allowable Subject Matter

8. Claims 6-8, 18, 19, 22 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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9. Applicant's arguments filed on 11/3/04, which have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chun Cao

Jan. 10, 2005